537,673

Rec'd PCT/PTO 06 JUN 2005

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

10/537673

(43) International Publication Date
24 June 2004 (24.06.2004)

PCT

(10) International Publication Number
WO 2004/054236 A1

(51) International Patent Classification[7]: H04N 3/233, 3/223

(21) International Application Number: PCT/IB2003/005606

(22) International Filing Date: 3 December 2003 (03.12.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/431,344 6 December 2002 (06.12.2002) US

(71) Applicant (*for all designated States except US*): **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(71) Applicant (*for AE only*): **U.S. PHILIPS CORPORATION** [US/US]; 1251 Avenue of the Americas, New York, NY 10510-8001 (US).

(72) Inventor; and
(75) Inventor/Applicant (*for US only*): **DE PAUW, Adriaan, Philippe, Digna** [NL/US]; 1109 McKay Drive, M/S-41SJ, San Jose, CA 95131 (US).

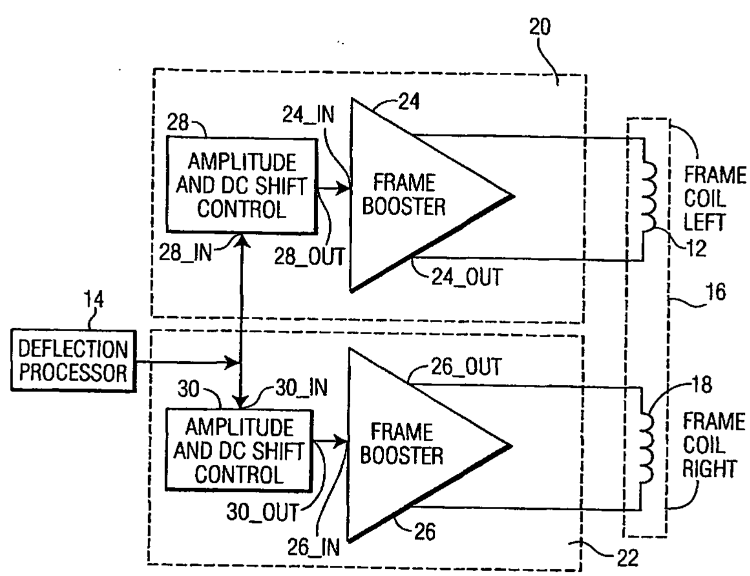
(74) Common Representative: **KONINKLIJKE PHILIPS ELECTRONICS N.V.**; c/o LESTER, Shannon, 1109 McKay Drive, M/S-41SJ, San Jose, CA 95131 (US).

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (*regional*): ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE,

[Continued on next page]

(54) Title: DRIVE APPARATUS FOR FRAME DEFLECTION AND METHOD



(57) Abstract: A frame drive circuit for a CRT device having a deflection processor (14) which develops a deflection processor output signal includes a frame coil (16) having a first core half (12) and a second core half (18), and a first driver (20) and a second driver (22). The deflection processor output signal is applied to each of the first driver (20) and the second driver (22). Each of the first driver (20) and the second driver (22) are selectively operative independently of each other to develop respectively a first coil drive signal (24 OUT) and a second coil drive signal (26 OUT) as a function of the deflection processor output signal. The first coil drive signal (24 OUT) and the second coil drive signal (26 OUT) are applied to a respective one of the first coil half (12) and said second coil half (18).

WO 2004/054236 A1

Rec'd PCT/PTO 06 JUN 2005

DRIVE APPARATUS FOR FRAME DEFLECTION AND METHOD

The present invention relates to deflection compensation, e.g. in Cathode Ray Tube (CRT) devices, e.g. monitors or televisions, and more particularly to a device and method for correcting various forms of deflection including rotation, trapezoidal and parallelogram deflection.

A CRT device forms an image using an electron beam focused on a fluorescent screen by electromagnetic deflection. The deflection is accomplished by applying current of sawtooth waveforms to horizontal and vertical coils.

A typical monitor is used as a peripheral device for a computer that provides video signals and horizontal and vertical sync signals necessary for forming an image at the monitor. An electron gun forms an electron beam according to the video signals. The electron beam is deflected in accordance with the horizontal and vertical sync signals horizontally and vertically by the horizontal and vertical coils on the fluorescent screen in front, thus representing a specified picture

The earth magnetic field influences deflection of electron beam by the horizontal and vertical deflecting coils, thus the picture is displayed on the screen in a monitor on the tilt to left or right. An additional coil is utilized in the prior art to complement for the tilt of the picture displayed by creating a complementing magnetic field. Such additional coil may be placed on the funnel portion of the tube used in the CRT device and the generated complementing magnetic field moves the tilt of the picture on the screen clockwise or counterclockwise, and the degree of tilt complement is variable.

However, the magnetic field created by the complementing coil may disadvantageously affect the quality of picture. Additionally, this implementation involves a problem that a special complement coil is required. Other prior art devices to correct for distortion are disclosed in U.S. Patent No.5,953,081, U.S. Patent No.5,686,800 and JP patent Publication 07-107503. Patent document US 5,953,081, incorporated herein by reference, discloses a system for correcting the tilt of a displayed picture due in part to the Earth magnetic field. In this document, the tilt of the picture can be controlled by controlling the tilts of the horizontal and vertical sawtooth waves applied to the horizontal and vertical coils respectively. Essentially horizontal and vertical parallelograms are simultaneously controlled by synthesizing the horizontal and vertical sawtooth waves, after controlling their amplitudes and phases with vertical and horizontal position control signals, respectively before sending them to a vertical output unit and a horizontal oscillation unit

thereby changing the tilt of the picture. In such implementation two respective sawtooth signals are applied to the respective horizontal and vertical coils. However the same sawtooth signal is applied to each of the two coils. Thus both halves of the horizontal and vertical coils are driven in series.

It is an object of the present invention to provide a novel apparatus and method that overcomes one or more limitations of the prior art hereinabove enumerated.

According to the present invention, a frame drive circuit for a device having a deflection processor which develops a deflection processor output signal includes a frame coil having a first core half and a second core half, and a first driver and a second driver. The deflection processor output signal is applied to each of the first driver and the second driver. Each of the first driver and the second driver are selectively operative independently of each other to develop respectively a first coil drive signal and a second coil drive signal as a function of the deflection processor output signal. The first coil drive signal and the second coil drive signal are applied to a respective one of the first coil half and said second coil half.

A feature of the present invention is that the existing frame coil such as the horizontal coil or the vertical coil, is split into separate core halves with each core half being separately driven, instead of in series as in the prior art. An advantage of the separate driving of the core halves is that greater design freedom is allowed, and correction of distortion may be accomplished without additional hardware, such as that disclosed in the prior art references.

These and other objects, advantages and features of the present invention will become readily apparent to those skilled in the art from a study of the following Description of the Exemplary Preferred Embodiments when read in conjunction with the attached Drawing and appended Claims.

Fig. 1 is a schematic diagram of a frame drive circuit constructed according to the principles of the present invention.

Fig. 2 is a representation of rotation correction accomplished by the present invention.

Fig. 3 is a representation of parallelogram correction accomplished by the present invention.

Fig. 4 is a representation of trapezoidal correction accomplished by the present invention.

Referring now to Fig.1, there is shown a frame drive circuit 10 for a CRT device such as a CRT monitor or a CRT television set and the drive circuit 10 includes a deflection processor 14 and a frame coil 16. According to the present invention, the frame drive circuit 10 includes a first core half 12 and a second core half 18 of the frame coil 16 and a first coil driver 20 and a second coil driver 22.

The deflection processor 14 develops, as is well know, a deflection processor output signal. The deflection processor output signal is applied to each of the first driver 20 and the second driver 22. Each of the first driver 20 and the second driver 22 are selectively operative independently of each other to develop respectively a first coil drive signal and a second coil drive signal as a function of the deflection processor output signal. The first coil drive signal and the second coil drive signal are in turn applied to a respective one of the first coil half 12 and the second coil half 18. As will be shown hereinafter, the two coil signals may differ in amplitude and one may be DC shifted relative to the other. The inventor has realized that applying different current to the two coils enables correcting the tilting of the picture without the need of an extra rotation coil used in some high-end CRT display system. The current difference enables correcting trapezoidal, rotational and parallelogram tilt of the picture. The adjustment of the respective coil currents may be effected at the time of manufacture of the display through testing or directly by the user during a tilt correction set up.

In one embodiment of the present invention, each of the first driver 20 and the second driver 22 amplify the deflection processor output signal to develop each respective one of the first coil drive signal and the second coil drive signal. In this embodiment, the amplification of the deflection processor output signal may be selected such that the resultant one of the first coil drive signal and the second coil drive signal when applied to the first coil half 12 and the second coil half 18, respectively, are operative to correct rotation of an image of the CRT monitor, as best seen in Fig.2.

In this embodiment the amplification of the deflection processor output signal by each of the first driver 20 and the second driver 22 may be substantially equal if the rotation of the CRT image is caused by a constant ambient field, such as the magnetic field of the earth. Furthermore, the ratio of the amplification of the deflection processor output signal may also be selectively adjusted to provide for trapezoidal correction, as best seen in Fig.4.

In another embodiment of the present invention, each of the first driver 20 and the second driver 22 further DC shift the deflection processor output signal to develop each

respective one of the first coil drive signal and the second coil drive signal. In this embodiment, the DC level shift of the deflection processor output signal may be selected such that the resultant one of the first coil drive signal and the second coil drive signal when applied to the first coil half 12 and the second coil half 18, respectively, are operative to parallelogram distortion of an image of the CRT monitor, as best seen in Fig.3.

It is contemplated by the present invention that the amplification of the deflection processor output signal, whether independently, in lockstep or in ratio, as well as the DC level shift, may all be utilized, alone or in any combination, in practicing the present invention. Usually, a CRT image will exhibit several forms of distortion, and correction of such distortion is accomplished by separate user settings for each type of distortion, as in the prior art. The present invention allows for the simplified apparatus to correct for several types of distortion simultaneously.

Accordingly each of the first driver 20 and the second driver 22 include an amplifier 24, 26 having an input 24_IN, 26_IN and an output 24_OUT, 26_OUT. The input 24_IN, 26_IN of each amplifier 24, 26 is adapted to receive the deflection processor output signal. The output 24_OUT, 26_OUT of each amplifier 24, 26 develops an amplified signal for application to a respective one of the first coil half 12 and the second coil half 18.

Each of the first driver 20 and the second driver 22 may further include a DC level shifter 28, 30 having respective inputs 28_IN, 30_IN and respective outputs 28_OUT, 30_OUT. The input 28_IN, 30_IN of each DC level shifter 28, 30 is adapted to receive the deflection processor output signal from the deflection processor 14. The output 28_OUT, 30_OUT of each DC level shifter 28, 30 develops a DC level shifted signal for application to a respective one of the first coil half 12 and the second coil half 18. The amplifier 24, 26 and the DC level shifter 28, 30 of each driver 20, 22 may be separate components connected in series or a single circuit, as seen in Fig. 1, that provides both functions.

There has been described hereinabove a novel frame drive circuit constructed according to the principles of the present invention. Those skilled in the art may now make numerous uses of, and departures from, the above-described embodiments without departing from the inventive concepts disclosed herein. Accordingly, the present invention is to be described solely by the lawfully permitted scope of the appended Claims.

CLAIMS

What is claimed is:

1. In a device having a deflection processor (14) developing a deflection processor output signal, a frame drive circuit comprising: a first driver (20) and a second driver (22), said deflection processor output signal being applied to each of said first driver (20) and said second driver (22), each of said first driver (20) and said second driver (22) being selectively operative independently of each other to develop respectively a first coil drive signal (24_OUT) and a second coil drive signal (26_OUT) as a function of said deflection processor output signal, said first coil drive signal (24_OUT) and said second coil drive signal (24_OUT) being applied to a respective one of a first coil half (12) and a second coil half (18) of a frame coil (16).

2. The frame circuit as set forth in Claim 1, wherein the device is a Cathode Ray Tube device comprising a horizontal coil and a vertical coil and the frame coil (16) is one of the horizontal coil or the vertical coil.

3. A frame drive circuit as set forth in Claim 1 wherein each of said first driver (20) and said second driver (22) amplify said deflection processor output signal to develop each respective one of said first coil drive signal (24_OUT) and said second coil drive signal (26_OUT).

4. A frame drive circuit as set forth in Claim 1 wherein each of said first driver (20) and said second driver (22) DC shift said deflection processor output signal to develop each respective one of said first coil drive signal (24_OUT) and said second coil drive signal (26_OUT).

5. A frame drive circuit as set forth in Claim 1 wherein each of said first driver (20) and said second driver (22) include an amplifier (24, 26) having an input (24_IN, 26_IN) and an output (24_OUT, 26_OUT), said input (24_IN, 26_IN) of each amplifier (24, 26) being adapted to receive said deflection processor output signal, said output (24_OUT, 26_OUT) of each amplifier (24, 26) developing an amplified signal for application to a respective one of said first coil half (12) and said second coil half (18).

6. A frame drive circuit as set forth in Claim 1 wherein each of said first driver (20) and said second driver (22) include DC level shifter (28, 30) having an input (28_IN, 30_IN) and an output (28_OUT, 30_OUT), said input (28_IN, 30_IN) of each DC level shifter (28, 30) being adapted to receive said deflection processor output signal, said output

(28_OUT, 30_OUT) of each DC level shifter (28, 30) developing DC level shifted signal for application to a respective one of said first coil half (12) and said second coil half (18).

7. A frame drive circuit of claim 1, wherein the circuit is comprised in an integrated circuit.

8. A method of correcting distortion of an image of a CRT monitor having a deflection processor (14) and a frame coil (16) comprising steps of: selectively developing independently of each other a first coil drive signal (24_OUT) and a second coil drive signal (26_OUT) as a function of a deflection processor output signal developed by said deflection processor; and applying said first coil drive signal (24_OUT) and said second coil drive signal (26_OUT) to a respective one of a first coil half (12) and a second coil half (18) of said frame coil (16).

9. A method as set forth in Claim 6, wherein said developing step includes amplifying said deflection processor output signal to develop each respective one of said first coil drive signal (24_OUT) and said second coil drive signal (26_OUT).

10. A method as set forth in Claim 6 wherein said developing step includes DC level shifting said deflection processor output signal to develop each respective one of said first coil drive signal (24_OUT) and said second coil drive signal (26_OUT).

11. A device comprising: a deflection processor (14) providing a deflection processor output signal; a frame coil (16), said frame coil having a first core half (12) and a second core half (18); a first driver (20) and a second driver (22), said deflection processor output signal being applied to each of said first driver (20) and said second driver (22), each of said first driver (20) and said second driver (22) being selectively operative independently of each other to develop respectively a first coil drive signal (24_OUT) and a second coil drive signal (26_OUT) as a function of said deflection processor output signal, said first coil drive signal (24_OUT) and said second coil drive signal (26_OUT) being applied to a respective one of said first coil half (12) and said second coil half (18).

Rec'd PCT/PTO 06 JUN 2005
10/537673
PCT/IB2003/005606

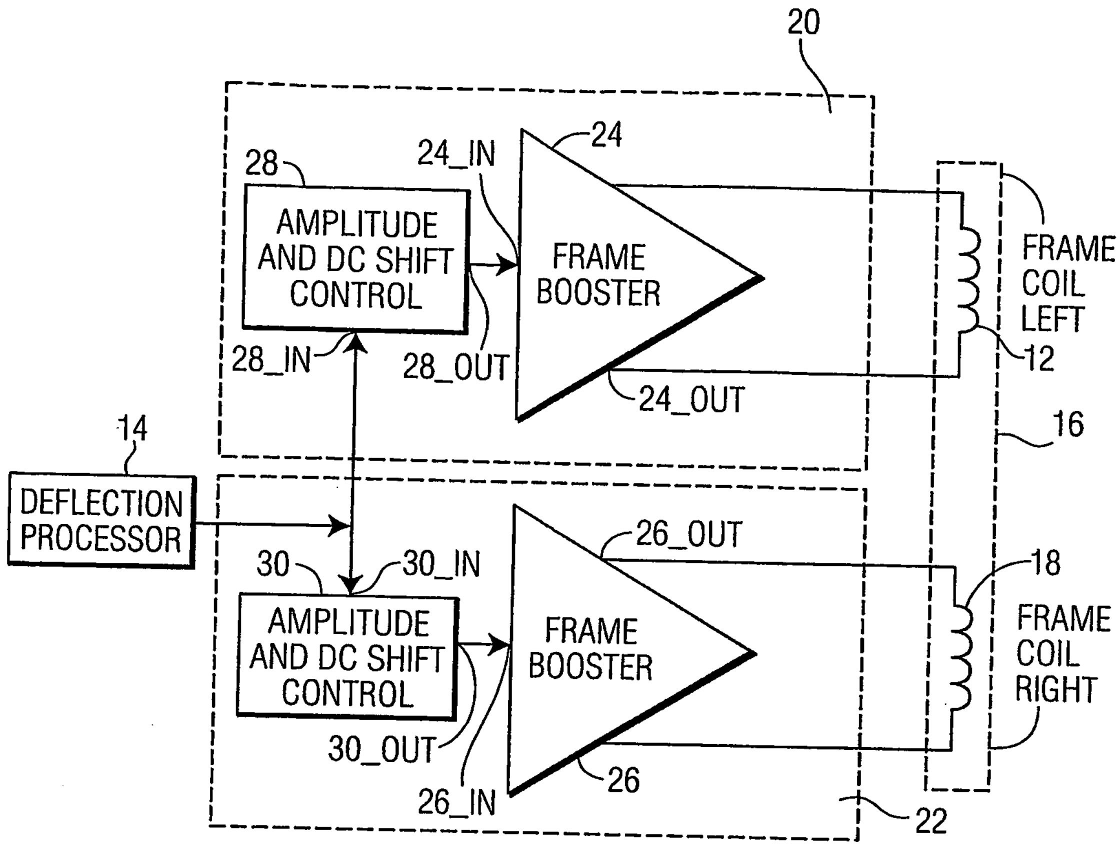


FIG. 1

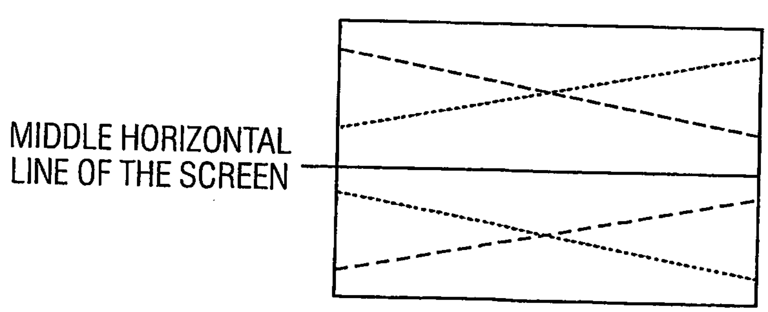


FIG. 2

Rec'd PCT/PTO 06 JUN 2005
10/537673

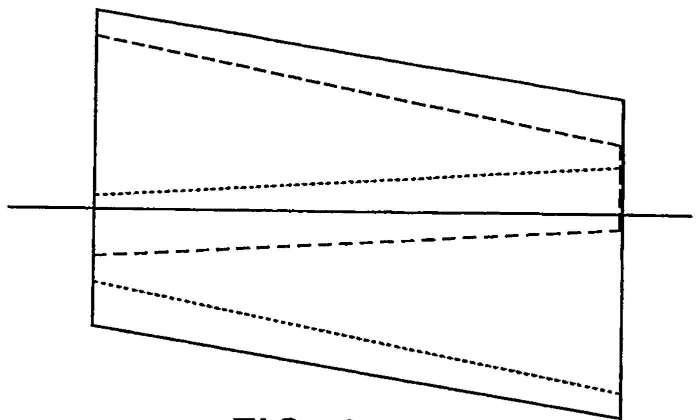


FIG. 3

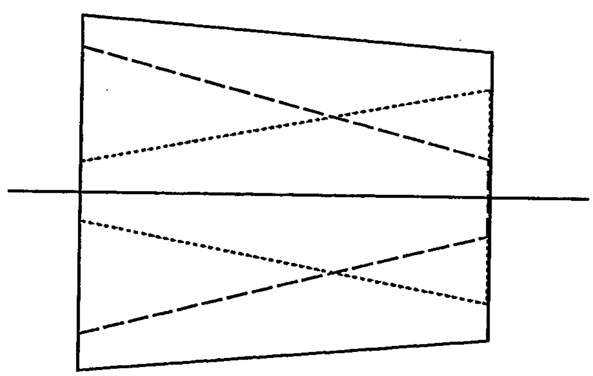


FIG. 4

INTERNATIONAL SEARCH REPORT

International Application No
PCT/IB 03/05606

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04N3/233 H04N3/223

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

PAJ, EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 2000, no. 25, 12 April 2001 (2001-04-12) & JP 2001 210255 A (TOTOKU ELECTRIC CO LTD), 3 August 2001 (2001-08-03) abstract ---	1,8,11
A	US 6 215 257 B1 (CHOE HWAN SEOK) 10 April 2001 (2001-04-10) column 2, line 18 - line 35; figures 6-8 ---	1,8,11
A	US 5 953 081 A (RYU JUN-YOUNG) 14 September 1999 (1999-09-14) cited in the application column 4, line 33 - line 58; figure 4 -----	1,8,11

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 February 2004	23/02/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Bequet, T

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/IB 03/05606

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 2001210255 A	03-08-2001	NONE	
US 6215257 B1	10-04-2001	CN 1220541 A	23-06-1999
		JP 2993957 B2	27-12-1999
		JP 11252578 A	17-09-1999
		TW 398011 B	11-07-2000
US 5953081 A	14-09-1999	KR 195907 B1	15-06-1999